Andes Technology and Arteris Partner To Accelerate RISC-V SoC Adoption

May 22, 2024

Highlights:

- Andes Technology and Arteris partnership aims to support the growing adoption of RISC-V SoCs by mutual customers.
- Focus is on high-performance/low-power RISC-V-based designs across a wide range of markets, including consumer electronics, communications, industrial applications and AI.
- The collaboration showcases integrated and optimized solutions with leading Andes RISC-V processor IPs and Arteris interconnect IP in silicon.

CAMPBELL, Calif., May 22, 2024 (GLOBE NEWSWIRE) -- Arteris, Inc. (Nasdaq: AIP), a leading provider of system IP that accelerates system-on-chip (SoC) creation and Andes Technology (TWSE: 6533), a founding and premier member of RISC-V International and a leading supplier of high-performance/low-power RISC-V processor IP, today announced their partnership to advance innovation for RISC-V based SoC designs for AI, 5G, networking, mobile, storage, AIoT and space applications.

The Andes QiLai RISC-V platform is a development board with a QiLai SoC featuring the Andes' RISC-V processor IPs along with Arteris FlexNoC interconnect IP used for on-chip connectivity. The QiLai SoC integrates the Andes 64-bit AX45MP multiprocessor (four cores in a cluster) running at 2.2 GHz and the NX27V vector processor running at 1.5 GHz, using Arteris network-on-chip (NoC) interconnect IP with subsystems for PCIe, DDR, SRAM and General Purpose IO using the AMBA AXI protocol. The supporting software includes the OpenSUSE Linux distribution, AndeSight™ toolchains, AndeSoft™ software stacks and AndesAIRE™ NN SDK to convert AI/ML models to executables

“Even though AndesCore™ AX45MP and NX27V processors are widely used, we are still pleased to see the QiLai SoC achieve first time right on new projects," said Dr. Charlie Su, Andes Technology's president and CTO. "Arteris NoC IP was the obvious choice for flexible, high-performance, top-level connectivity across the QiLai SoC. The QiLai platform enhances the rapid development and assessment of RISC-V software, accelerating the expansion of the RISC-V ecosystem."

"We are excited to partner with Andes Technology and support the QiLai platform interoperability to further accelerate RISC-V technology mainstream adoption," said Michal Siwinski, chief marketing officer at Arteris. "Our collaboration supports our mission to be the catalyst for SoC innovation so our mutual customers can focus on efficiently creating tomorrow's breakthroughs."

Arteris' FlexNoC non-coherent NoC IP and Ncore cache-coherent NoC IP enable scalable, low latency and power-efficient on-chip communication to achieve superior performance in complex SoC designs. The technology facilitates the integration of high-performance, low-power CPU IPs, enhancing system functionality and interoperability, especially within the growing RISC-V ecosystem. This configurable and adaptable interconnect solution seamlessly interfaces with various components to mitigate risks and expedite time to market. By connecting well-tested CPU IP blocks, system designers can leverage Arteris NoC IPs to enhance the reliability and quality of next-generation SoCs.

Customers can request a devkit featuring the Andes QiLai RISC-V platform at sales@andestech.com. For more information on the partnership and respective products, please contact info@arteris.com and info@andestech.com.

About Arteris

Arteris is a leading provider of system IP for accelerating system-on-chip (SoC) development across today's electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration automation technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

About Andes Technology

Nineteen years in business and a founding premier member of RISC-V International, Andes is a publicly-listed company (TWSE: 6533; SIN: US03420C2089; ISIN: US03420C1099) and a leading supplier of high-performance/low-power 32/64-bit embedded processor IP solutions, and the driving force in taking RISC-V mainstream. Its V5 RISC-V CPU families range from tiny 32-bit cores to advanced 64-bit Out-of-Order processors with DSP, FPU, Vector, Linux, superscalar, functional safety and/or multi/many-core capabilities. By the end of 2023, the cumulative volume of Andes-Embedded™ SoCs has surpassed 14 billion. For more information, please visit https://www.andestech.com. Follow Andes on LinkedIn, Twitter, Bilibili and YouTube!

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