**ARTERIS** IP

# Arteris Expands Automotive Solutions for Armv9 Architecture CPUs

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Highlights:

- Arteris delivers on previously announced collaboration with Arm to speed up automotive electronics innovation with an emulation-based validation system for Armv9 and CHI-E based designs.

- Arteris aligned roadmap with Arm to enable designers to get to market faster with an optimized and pre-validated high-bandwidth, low-latency Ncore cache coherent interconnect IP for Arm's Automotive Enhanced (AE) compute portfolio.

- Collaboration integrates Arm processors with Arteris interconnect IP to enable autonomous driving, advanced driver-assistance systems (ADAS), cockpit and infotainment, vision, radar and lidar, body and chassis control, zonal controllers and other automotive applications.

CAMPBELL, Calif., March 13, 2024 (GLOBE NEWSWIRE) -- Arteris, Inc. (Nasdaq: AIP), a leading provider of system IP which accelerates system-on-chip (SoC) creation, today announced the first deliverables of its ongoing partnership with Arm to speed up automotive electronics innovation based on the latest generation of Arm® Automotive Enhanced (AE) technologies. The collaboration integrates Armv9-based Cortex® processors with Arteris system IP to enable autonomous driving, advanced driver-assistance systems (ADAS), cockpit and infotainment, vision, radar and lidar, body and chassis control, and other automotive applications.

"We are at an inflection point in the automotive industry that requires a fundamental rethink of automotive product development and deployment methodologies," said Suraj Gajendra, vice president of products and solutions, Automotive Line of Business, Arm. "The latest generation of Arm Automotive Enhanced compute and software solutions, integrated with Arteris' flexible and configurable Ncore cache coherent interconnect IP, means customers can begin development sooner, accelerating time to market for next-generation vehicle electronics."

Arteris has optimized and pre-validated its high-bandwidth, low-latency Ncore cache coherent interconnect IP including its safety capabilities with Arm Cortex-A cores, DynamIQ Shared Units (DSUs) and Generic Interrupt Controller (GIC) using hardware emulation to ensure interoperability. The resulting validation system boots Linux on a multi-cluster Arm design and executes test suites to validate critical cache coherency cases. This ultimately accelerates the path for customers to realize SoCs with high performance and power efficiency for complex and demanding safety-critical tasks with differing workloads while reducing project schedules and costs.

Arteris Ncore cache coherent interconnect IP offers unique flexibility and configurability to allow user-defined configurations for heterogenous topologies, supporting CHI-B, CHI-E, ACE and AXI protocols. It seamlessly integrates with the Arteris non-coherent FlexWay interconnect IP and physically aware FlexNoC 5 interconnect IP.

"Customers are always looking to accelerate the pace of innovation and the Arm Automotive-Enhanced compute portfolio provides the foundation needed to address advanced automotive electronics requirements," said Frank Schirrmeister, vice president of solutions and business development of Arteris. "Through our expanded collaboration with Arm, customers using Arteris system IP benefit from improved productivity and faster time to tapeout."

**About Arteris**
Arteris is a leading provider of system IP for accelerating system-on-chip (SoC) development across today's electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration automation technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

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