Arteris Unveils Next-Generation FlexNoC 5 Physically Aware Network-on-Chip IP

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Highlights:

- *5th generation of network-on-chip interconnect silicon IP technology*
- *Up to 5X faster physical convergence vs manual physical iterations*
- *Enables customers to achieve PPA goals within schedule and budget constraints*

CAMPBELL, Calif., Feb. 22, 2023 (GLOBE NEWSWIRE) -- Arteris, Inc. (Nasdaq: AIP), a leading provider of system IP which accelerates system-on-chip (SoC) creation, today announced the launch of Arteris FlexNoC 5 physically aware network-on-chip (NoC) interconnect IP. FlexNoC 5 enables SoC architecture teams, logic designers and integrators to incorporate physical constraint management across power, performance and area (PPA) to deliver a physically aware IP connecting the SoC. This technology enables 5X faster physical convergence over manual refinements with fewer iterations from the layout team for automotive, communications, consumer electronics, enterprise computing, and industrial applications.

Manual workflows typically include numerous iterations of pipeline insertions, effort-intensive creation of constraints for physical placement of units, and lengthy NoC placement plus route iterations to converge on the SoC PPA targets. By contrast, FlexNoC 5 physical awareness eliminates these iterations and shortens the duration of various manual steps, facilitating up to 5X faster physical convergence of the back-end physical design time and effort. The resulting physically optimized NoC IP instance is then ready for output to physical synthesis and place and route for implementation.

“Sondrel has deployed Arteris FlexNoC interconnect IP across several customer SoC projects to great effect,” said Graham Curren, CEO of Sondrel. “Physical constraints have always been an important issue and are even more important below 16nm geometries. The latest FlexNoC 5 with its physical awareness technology, enables our RTL teams to verify that architectures meet physical constraints and provide a better starting point for our place and route team. We look forward to our continued cooperation with Arteris.”

Moreover, FlexNoC 5 expands support for Arm AMBA 5 protocols and IEEE 1685 IP-XACT, including a connectivity flow with Arteris Magillem for NoC integration with other SoC IP blocks. FlexNoC 5 also supports the production-proven Arteris resilience option for automotive functional safety qualification and data center reliability, the advanced memory option for optimizing memory traffic, and the Arteris option for very large designs. For more information on FlexNoC 5, please visit arteris.com/flexnoc.

“Without physical awareness, it is quite possible to develop SoC architectures that are difficult or even impossible to place and route resulting in multiple turns, overall project delay risks, and additional project costs, particularly for geometries of 16nm and below,” said K. Charles Janac, president and CEO of Arteris. “With FlexNoC 5, we consider physical effects early in the process, delivering physically aware NoC IP which helps customers meet PPA goals and execute SoC projects on schedule and budget.”

About Arteris

Arteris is a leading provider of system IP for the acceleration of system-on-chip (SoC) development across today’s electronic systems. Arteris network-on-chip (NoC) interconnect IP and IP deployment technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

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