Arteris® IP Helps Automate System-on-Chip Semiconductor Design Traceability with Harmony Trace™ Design Data Intelligence

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Enterprise-level server-based application increases system quality and enables faster Functional Safety Certifications by creating and maintaining traceability between different systems

CAMPBELL, Calif., Nov. 16, 2021 (GLOBE NEWSWIRE) -- Arteris IP (NASDAQ: AIP), a leading provider of system-on-chip (SoC) system IP consisting of network-on-chip (NoC) interconnect and IP deployment software that accelerate SoC creation, today announced the launch of the Arteris® Harmony Trace™ Design Data Intelligence Solution to ease compliance with semiconductor industry functional safety and quality standards such as ISO 26262, IEC 61508, ISO 9001, and IATF 16949.

Highlights of this Announcement:

- Harmony Trace increases system quality and accelerates functional safety assessments by identifying and fixing the traceability gaps between disparate systems.
- Harmony Trace is implemented as an enterprise-level server-based application with a web-based user interface (UI).
- Harmony Trace is unique because it gives engineers the freedom to use the “best tool for the job” and automates linking requirements and artifacts.

For design teams with functional safety requirements or who create complex SoCs or systems, Arteris® Harmony Trace™ increases system quality and the ability to achieve functional safety certifications. By creating and maintaining traceability between disparate systems for requirements, specifications, EDA and hardware designs, software code, and documentation, engineers will know immediately when a change occurs and the effect of that change on other design artifacts and parts of the system.

Harmony Trace is implemented as an enterprise-level server-based application with a web-based UI that interfaces with EDA, documentation, existing requirements, software engineering and support systems. Unlike Application Lifecycle Management (ALM) and Product Lifecycle Management (PLM) solutions that require engineers to use a single environment that is not best-in-class in any one aspect, Arteris Harmony Trace creates a system-of-systems that allows complete visibility of requirements traceability through the entire SoC design flow and product life cycle.

“Developing a complex SoC often involves a suite of disparate and disconnected tools, which makes it difficult to maintain a record that allows tracing design requirements and artifacts over the product’s lifetime,” said Mike Demler, senior analyst at The Linley Group. “But Arteris Harmony Trace mitigates these issues by connecting discrete silos such that users can track requirements, implementation, verification and documentation mismatches across existing systems. This means that engineers can continue to use best-in-class solutions and technologies like EDA tools, IBM DOORS, Jama, Jira, DITA, and IP-XACT while experiencing the benefits of automated traceability. Harmony Trace helps design teams meet the quality and change management requirements of functional safety standards such as ISO 26262 and IEC 61508.”

“The development of Arteris Harmony Trace was driven by our customers’ needs to establish an automated traceability flow and implement change management best practices between their existing requirements, specification, EDA, code repository and documentation tools,” said K. Charles Janac, president and CEO of Arteris IP. “Harmony Trace allows our customers to use their existing tools and automatically link data between them due to its unique semiconductor industry-specific semantic computing technology.”

About Arteris IP

Arteris IP (NASDAQ: AIP) provides system-on-chip (SoC) system IP consisting of network-on-chip (NoC) interconnect IP and IP deployment technology to accelerate system-on-chip (SoC) semiconductor development and integration for a wide range of applications from AI to automobiles, mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Bosch, Baidu, Mobileye, Samsung, Toshiba and NXP. Arteris IP products include the Ncore® cache coherent interconnect IP and FlexNoC® non-coherent interconnect IP, the CodaCache® standalone last level cache, and optional Resilience Package (ISO 26262 functional safety), FlexNoC AI Package, and PIANO® automated timing closure capabilities. Our IP deployment products provide intelligent automation that accelerates the development and increases the quality of SoC hardware designs and their associated software and firmware, verification and simulation platforms, and specifications and customer documentation. Customer results obtained by using Arteris IP products include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at https://www.linkedin.com/company/arteris.

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A video accompanying this announcement is available at https://www.globenewswire.com/NewsRoom/AttachmentNg/835e9c39-4d67-4fe7-9aff-fcc4bccd6ee7

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