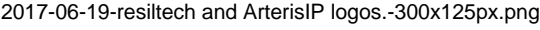




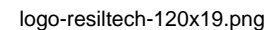
## ArterisIP and ResilTech Announce Strategic Partnership to Facilitate ISO 26262 Compliance for Complex Autonomous Automotive Systems

June 20, 2017

Joint engineering and integration effort simplifies and accelerates ISO 26262 FMECA and diagnostic coverage for ASIL D qualification

CAMPBELL, Calif. and PONTEDERA, Italy — June 202017 — ArterisIP, the innovative supplier of silicon-proven commercial system-on-chip (SoC) interconnect IP, and ResilTech S.R.L., the leader in resilient computing and functional safety for automotive systems, today announced a strategic partnership to help semiconductor design teams efficiently validate ISO26262 functional safety levels for automotive systems-on-chip. 

*"Working with ArterisIP allows ResilTech to apply its automotive resilience expertise to a broad range of automotive SoC projects. Our goal is to not only provide interconnect-specific functional safety knowledge to ArterisIP automotive customers, but to also ultimately facilitate a resilience verification solution for highly complex SoCs."*



Andrea Bondavalli, Senior Board Member and Co-Founder, **ResilTech**

The growth in supercomputer-like performance required for city-driving autonomous vehicles is causing explosive adoption of highly parallel chip architectures using [cache coherency](#) for machine learning, computer vision and sensor fusion. This, in turn, magnifies the complexity of functional safety mechanisms and diagnostic coverage analyses required to achieve the ISO 26262 ASIL D level. Both companies think that for full commercial deployment, automated driving electronics will require ASIL D functional safety level certification. Because these SoC architectures are implemented in the physical world through the configuration of inter-processor communications, the on-chip SoC interconnect bears the burden of simultaneously satisfying these conflicting requirements.

[DOWNLOAD NCORE PAPER BY LINLEY GROUP \(MPR\)](#)

The ArterisIP and ResilTech partnership addresses these issues by providing SoC designers:

- A quantitative (FMECA) and qualitative (FMEA) functional safety assessment of the [ArterisIP Ncore Cache Coherent Interconnect](#) and the [Ncore Resilience Package IP](#)
- A complete set of ISO 26262 deliverables for multiple SoC reference designs, which can then be used as a foundation for design teams to prepare ISO 26262 work products for their own custom SoC designs
- Tools and methods to automate this work, including directing fault injection campaigns using industry-leading EDA tools
- Consulting services by experienced functional safety and interconnect IP experts to help ArterisIP and ResilTech customers more quickly perform their own ISO 26262 activities

"Working with ArterisIP allows ResilTech to apply its automotive resilience expertise to a broad range of automotive SoC projects," said Andrea Bondavalli, Senior Board Member and Co-Founder of ResilTech. "Our goal is to not only provide interconnect-specific functional safety knowledge to ArterisIP automotive customers, but to also ultimately facilitate a resilience verification solution for highly complex SoCs."

"We are excited to be working with ResilTech to accelerate ISO 26262 functional safety analyses for automotive semiconductor designers creating the world's most advanced autonomous driving SoCs," said K. Charles Janac, President and CEO of ArterisIP. "A key objective of our partnership with ResilTech is to build a highly productive functional safety ecosystem for our mutual customers."

### About ArterisIP

ArterisIP provides [system-on-chip \(SoC\) interconnect IP](#) to accelerate SoC semiconductor assembly for a wide range of applications from IoT to mobile phones, cameras, automobiles, SSD controllers and servers for customers such as [Samsung](#), [Huawei / HiSilicon](#), [Mobileye](#), [Altera](#) (Intel), and [Texas Instruments](#). ArterisIP products include the [Ncore](#) cache coherent and [FlexNoC](#) non-coherent interconnect IP, as well as optional [Resilience Package \(functional safety\)](#) and [PIANO automated timing closure](#) capabilities. Customer results obtained by using the ArterisIP product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit [www.arteris.com](http://www.arteris.com) or find us on LinkedIn at [www.linkedin.com/company/arteris](http://www.linkedin.com/company/arteris).

## **About ResilTech**

Resiltech provides services and solutions to ensure the safety and resilience of electronic and computer based solutions to a variety of critical applications and domains including Railways, Metrolines, Automotive and Industrial. Experts from Resiltech join the activity of the ISO Working Group developing the Automotive Functional Safety standard ISO 26262 since the first edition (2011), and now they are involved in the second edition (2018). The support and solutions (based on own methodologies and automated processes and tooling) for Safety management, Safety processes definitions, Requirement Management, Hazard analysis, HW and SW Safety analysis, SoC level HW analysis of micro-architectures, Design/ development/ verification of STL (self test libraries) for CPUs, RAM and Pheripherals, FMEA and FMEDA have made Resiltech a competent and key partner to many actors in Automotive Safety. For more information see <http://www.resiltech.com/>.

## **Editorial Contacts**

Kurt Shuler  
ArterisIP  
+1 408 470 7300  
[kurt.shuler@arteris.com](mailto:kurt.shuler@arteris.com)

Francesco Rossi  
ResilTech  
+39 0587-212465  
[francesco.rossi@resiltech.com](mailto:francesco.rossi@resiltech.com)

*Arteris, ArterisIP, FlexNoC, Ncore, PIANO, and the ArterisIP logo are trademarks of Arteris, Inc. All other product or service names are the property of their respective owners.*