




## Ty Garibay joins ArterisIP as Chief Technology Officer

September 5, 2017

CAMPBELL, Calif. — September 5 2017 — ArterisIP, the innovative supplier of silicon-proven commercial [system-on-chip \(SoC\) interconnect IP](#), today announced the appointment of Ty Garibay as ArterisIP's Chief Technology Officer (CTO). Mr. Garibay will play a key role in extending ArterisIP's innovation leadership in the on-chip interconnect semiconductor IP market, molding the company's technical vision and driving corporate technology strategy as the industry adapts to serve the need for functionally safe machine learning and [autonomous driving systems](#). 

"Ty is a highly respected technologist with a strong reputation and an excellent depth of knowledge in on-chip communications, SoC architecture and IC design. He is a well-known industry thought leader with a proven track record of semiconductor innovation, deep customer relationships and breakthrough product definition," said K. Charles Janac, President and CEO of ArterisIP. "We are delighted to have Ty join us as we drive to continue our undisputed leadership in on-chip communications and interconnect IP."

*"As a long-time ArterisIP customer and partner, I am excited to have the opportunity to contribute directly to the company's success. The ArterisIP team has established themselves as not only the leading provider of commercial network-on-chip based interconnect IP, but also as a trusted technology partner to most of the world's leading SoC design teams. I look forward to carrying on this tradition of excellence as part of this highly skilled team."*

ArterisIP-logo-col-white-182px.png  
Ty Garibay, Chief Technology Officer, **ArterisIP**

Mr. Garibay has played key roles in the development of microprocessor and system-on-chip architectures and technologies, serving in architect and design leadership roles at Motorola, Cyrix, SGI, and Alchemy Semiconductor. He managed ARM's Austin Design Center and also ARM cores development and IC engineering for Texas Instruments' OMAP application processors group. Most recently, Mr. Garibay was Vice President of IC Engineering for Altera, and later led FPGA IC design at Intel after it acquired Altera in late 2015. Mr. Garibay has authored and co-authored 34 patents, and has been published in multiple technical journals and conferences.

"As a long-time ArterisIP customer and partner, I am excited to have the opportunity to contribute directly to the company's success," said Ty Garibay, CTO of ArterisIP. "The ArterisIP team has established themselves as not only the leading provider of commercial network-on-chip based interconnect IP, but also as a trusted technology partner to most of the world's leading SoC design teams. I look forward to carrying on this tradition of excellence as part of this highly skilled team."

A high-resolution [photograph of Garibay](#) can be found [here](#) at the ArterisIP website.

### About ArterisIP

ArterisIP provides [system-on-chip \(SoC\) interconnect IP](#) to accelerate SoC semiconductor assembly for a wide range of applications from IoT to mobile phones, cameras, automobiles, SSD controllers and servers for customers such as [Samsung](#), [Huawei / HiSilicon](#), [Mobileye \(Intel\)](#), [Altera \(Intel\)](#), and [Texas Instruments](#). ArterisIP products include the [Ncore](#) cache coherent and [FlexNoC](#) non-coherent interconnect IP, as well as optional [Resilience Package \(ISO 26262 functional safety\)](#) and [PIANO automated timing closure](#) capabilities. Customer results obtained by using the ArterisIP product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit [www.arteris.com](http://www.arteris.com) or find us on LinkedIn at [www.linkedin.com/company/arteris](http://www.linkedin.com/company/arteris).

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