ArterisIP Ncore Cache Coherent Interconnect and Resilience Package Licensed by NXP

September 19, 2017

CAMPBELL, Calif. —September 19, 2017 — ArterisIP, the innovative supplier of silicon-proven commercial system-on-chip (SoC) interconnect IP, today announced that NXP Semiconductors has licensed additional uses of Ncore Cache Coherent Interconnect IP and Ncore Resilience Packages.

> *"We had an excellent experience implementing ArterisIP's Ncore Cache Coherent Interconnect IP in our previous SoC developments so we have chosen to expand the adoption of this technology for our next generation SoCs.*

NXP-Logo-arteris-182x66.png

Benny Chang, Vice President of R&D, Automotive MCU and Processors Business Line, ***NXP Semiconductors***

DOWNLOAD NCORE PRESENTATION

NXP originally participated with ArterisIP in the Ncore product launch in May 2016. This license facilitates additional uses of the new Ncore version 2.0 IP as well as new Ncore Resilience Packages. In addition, NXP has been a long-term user of the FlexNoC non-coherent interconnect and has licensed additional uses of the FlexNoC IP and the FlexNoC Resilience Packages.

"We had an excellent experience implementing ArterisIP's Ncore cache coherent interconnect IP in our previous SoC developments so we have chosen to expand the adoption of this technology for our next generation SoCs," said Benny Chang, Vice President of R&D for NXP's Automotive MCU and Processors Business Line. "The addition of the Ncore Resilience Packages offers capabilities that help us make chips that are extremely complex and can be proven to be functionally safe up to ASIL D level for coherent as well as non-coherent parts of our SoCs."

The Ncore Resilience Packages provide integrated interconnect hardware data protection and intelligent unit duplication to detect and report system faults. The Ncore Resilience Package includes a functional safety controller with advanced Built-In Self-Test (BIST) as well as a complete ISO 26262 safety package with documentation.

"Simultaneous implementation of heterogeneous cache coherency while meeting ISO 26262 functional safety requirements demands the use of state-of-the-art on-chip interconnect technologies tailored for the unique needs of complex autonomous driving SoCs," said K. Charles Janac, President and CEO of Arteris. "We are delighted that the automotive design teams at NXP Semiconductors trust ArterisIP to provide these necessary capabilities."

About ArterisIP

ArterisIP provides system-on-chip (SoC) interconnect IP to accelerate SoC semiconductor assembly for a wide range of applications from automobiles to mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Samsung, Huawei / HiSilicon, Mobileye (Intel), Altera (Intel), and Texas Instruments. ArterisIP products include the Ncore cache coherent and FlexNoC non-coherent interconnect IP, as well as optional Resilience Package (ISO 26262 functional safety) and PIANO automated timing closure capabilities. Customer results obtained by using the ArterisIP product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at www.linkedin.com/company/arteris.

Editorial Contact

Kurt Shuler
Arteris Inc.
+1 408 470 7300
kurt.shuler@arteris.com