ArterisIP announces Ncore 3 Cache Coherent Interconnect

October 4, 2017

Enables next-generation machine learning and autonomous driving SoCs with support for Arm AMBA CHI protocol, CCIX, and ISO 26262 Functional Safety

Linley Processor Conference 2017, SANTA CLARA, Calif. —October 4, 2017 — ArterisIP, the innovative supplier of silicon-proven commercial system-on-chip (SoC) interconnect IP, today announced the Ncore Cache Coherent Interconnect IP version 3 along with the optional Ncore Resilience Package for functional safety.

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> zte-logo-arteris-1.jpg
> *Mr. Yu Li, Vice President , **ZTE (SaneChips)***

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Ncore 3 is a distributed heterogeneous cache coherent on-chip interconnect that enables SoC design teams to integrate processor clusters using the latest Arm® AMBA® CHI protocol (CHI Issue B). Key benefits include:

1. Uniquely, Ncore 3 allows both AMBA CHI and ACE processor clusters and accelerators to operate as fully coherent peers in the same chip, giving design teams flexibility in choosing CPU and hardware accelerator IP. The ArterisIP CHI interface includes support for high level coherency semantics such as Atomics and Cache Stashing used by high-performance SoCs.
2. The Ncore Cache Coherent Interconnect for Accelerators (CCIX) controller enables easy scaling of coherent systems across multiple chips via the Synopsys® DesignWare® Controller and PHY IP for PCI Express® and CCIX.
3. To enable advanced systems targeted at the automotive market, the Ncore 3 product line also includes the optional Ncore Resilience Package. This package accelerates customers' ISO 26262 certification by offering: (1) ISO 26262-compliant in-hardware functional safety mechanisms, and (2) a complete set of functional safety analyses and documentation.

"As current users of the Ncore cache coherent interconnect, we are excited about the technical innovation in ArterisIP's new Ncore 3 IP," said Mr. Yu Li, Vice President at Sanechips Technology Co. Ltd, the semiconductor subsidiary of ZTE. "Enabling both the AMBA CHI and ACE protocols in the same SoC will allow for greater use of existing IP in high-performance systems."

The Ncore 3 Cache Coherent Interconnect IP is ideally suited for "supercomputer-on-a-chip" applications, such as those required for autonomous driving controllers and advanced driving assistance systems (ADAS), machine learning applications, server / data center processing, and networking. Ncore's highly configurable, distributed architecture allows design teams to more easily create complex systems that are more optimized for stringent power consumption, performance, and area requirements.

"Development of Ncore 3 was driven by our customers' desires to create large-scale high-performance computing and machine learning systems that conform to an embedded system's power consumption and area requirements," said K. Charles Janac, President and CEO of Arteris. "Ncore 3.0 interconnect IP builds on our proven Ncore cache coherent interconnect technology to implement functional safety features with Arm AMBA CHI protocol processors, permitting the entire SoC to be more easily qualified for ISO 26262 ASIL D for use in autonomous driving systems."

Supporting Quotations:

Arm

"ArterisIP's support of the Arm AMBA CHI cache coherent protocol shows the choice and richness of the Arm ecosystem," said Javier Orensanz, general manager, Development Solutions Group, Arm. "The development of AMBA-compliant technologies, like the Ncore 3 Interconnect, and the long-term agreement between Arm and ArterisIP to provide access to Arm Cycle Models of CPU and system IP, demonstrates continued support for the design, verification, and optimization of high-performance cache coherent subsystems for the benefit of our ecosystem partners."

Synopsys

"Synopsys' DesignWare CCIX IP, taped out in the 7-nm FinFET process, provides designers with a low-risk solution that interoperates seamlessly with the ArterisIP Ncore interconnect," said John Koeter, Vice President of Marketing for IP at Synopsys. "Our CCIX Controller and PHY IP, based on Synopsys' silicon-proven PCI Express architecture which has been used in over 1,500 designs and shipped in billions of units, enables our mutual

customers to confidently integrate the IP into their SoCs."

CCIX Consortium

"CCIX enables a new class of interconnect for emerging acceleration applications in the datacenter," said Gaurav Singh, chairman of the CCIX Consortium. "We are pleased to see ArterisIP taking a leading role to accelerate CCIX adoption among our member companies."

ResilTech

"Systems-on-chip for autonomous driving are becoming more complex, often requiring cache coherence and integrating multiple types of processor clusters and hardware accelerators," said Andrea Bondavalli, Professor of Computer Science and head of the Resilient Computing Lab at the University of Florence, and scientific advisor to ResilTech, a leading functional safety consultancy. "The ArterisIP Ncore cache coherent interconnect not only allows the construction of these new automotive SoCs, but also implements safety mechanisms in hardware that increase the functional safety diagnostic coverage of the entire SoC. ArterisIP technology thus allows design teams to create highly complex SoCs that are capable of meeting the ISO 26262 ASIL D classification."

Availability

The Ncore 3 Cache Coherent Interconenct IP and Ncore Resilience Package are available for early access customers in November 2017.

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About ArterisIP

ArterisIP provides system-on-chip (SoC) interconnect IP to accelerate SoC semiconductor assembly for a wide range of applications from automobiles to mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Samsung, Huawei / HiSilicon, Mobileye (Intel), Altera (Intel), and Texas Instruments. ArterisIP products include the Ncore cache coherent and FlexNoC non-coherent interconnect IP, as well as optional Resilience Package (ISO 26262 functional safety) and PIANO automated timing closure capabilities. Customer results obtained by using the ArterisIP product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at www.linkedin.com/company/arteris.

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