Arteris IP and Synopsys Accelerate the Optimization of Heterogeneous Multicore Neural Network Systems-on-Chip

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Ncore Cache Coherent Interconnect IP and Synopsys Platform Architect fast-tracks integration for autonomous driving and artificial intelligence (AI) markets

CAMPBELL, Calif. — January 30, 2018 — Arteris IP, the innovative supplier of silicon-proven commercial system-on-chip (SoC) interconnect IP, today announced the integration of its Ncore Cache Coherent IP with the Synopsys® Platform Architect™ virtual prototyping solution to provide designers of neural network and autonomous driving SoCs with the ability to analyze system-level performance and power consumption earlier in the design cycle for their next-generation multicore architectures.

> *"Combining Platform Architect and Ncore System models provides designers with the ability to analyze and optimize an entire heterogeneous multicore SoC architecture before RTL is available.*
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> *Eshel Haritan, Vice President of R&D, Verification Group,* ***Synopsys***

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"As we collaborate with industry leaders developing neural network and autonomous driving SoCs, we know first-hand that teams must quickly validate candidate architectures as early as possible, and then optimize them for performance and power consumption," said Eshel Haritan, vice president of R&D in the Synopsys Verification Group. "These architectures can use different combinations of hardware accelerators, and analysis requires state-of-the-art simulation. Combining Platform Architect and Ncore System models provides designers with the ability to analyze and optimize an entire heterogeneous multicore SoC architecture before RTL is available."

Artificial Intelligence (AI) and autonomous driving systems require multiple heterogeneous processing elements connected using complex caching, interconnect and memory architectures, all of which are challenging to analyze, optimize, and tune. The integration of Ncore IP with Platform Architect provides system architects with a fast and accurate simulation model of Arteris Ncore Cache Coherent IP, allowing them to make smart architectural trade-off decisions based on the deep visibility that the model provides. Ncore IP has been quickly adopted by automotive and AI leaders such as NXP, Toshiba, and others. Close integration of the products and design flows developed by Arteris IP and Synopsys will continue to benefit the greater SoC market.

The Arteris Ncore IP and Synopsys Platform Architect integration provides the following benefits for system design teams:

- **Earlier architecture exploration for performance and power**. Arteris' Ncore interconnect models in Synopsys' Platform Architect enable early architecture analysis and optimization of performance and power before system RTL is available
- **Unparalleled visibility into Ncore interconnect internal states,** which allows detailed system-wide analysis of resource utilization (e.g., snoop filters, cache hits/misses) and interconnect metrics (e.g., bandwidth, latency)
- **Industry-leading interconnect model performance and flexibility**. Sub-16nm systems are large and complex; the Ncore SystemC model is highly optimized for simulation performance, enabling exploration of hundreds of design options with quick turnaround time

"Our integration with Synopsys Platform Architect provides Ncore users with incomparable visibility into the internals of the highly configurable Ncore interconnect IP, delivering to architects and design teams detailed knowledge about their systems that can then be used for performance exploration, optimization and validation," said Joe Butler, Vice President of Engineering at Arteris IP. "Our joint engineering work with Synopsys has resulted in a combined solution that eases architecture, design, and configuration of complex heterogeneous multicore SoCs."

About Arteris IP

Arteris IP provides system-on-chip (SoC) interconnect IP to accelerate SoC semiconductor assembly for a wide range of applications from automobiles to mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Samsung, Huawei / HiSilicon, Mobileye (Intel), Altera (Intel), and Texas Instruments. Arteris IP products include the Ncore cache coherent and FlexNoC non-coherent interconnect IP, as well as optional Resilience Package (functional safety) and PIANO automated timing closure capabilities. Customer results obtained by using the Arteris product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at https://www.linkedin.com/company/arteris.

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