Arteris IP FlexNoC® Interconnect IP Licensed by Iluvatar CoreX for Artificial Intelligence Application

October 18, 2018

CAMPBELL, Calif. – October 16, 2018– Arteris IP, the leading supplier of innovative, silicon-proven network-on-chip (NoC) interconnect intellectual property, today announced that Iluvatar CoreX has licensed Arteris IP FlexNoC Interconnect for a deep learning SoC application. Iluvatar CoreX is a company focused on designing high-end / cloud computing chips and computing infrastructure software, with R&D centers in Nanjing, Shanghai, Beijing, and Silicon Valley.

> *"We chose the Arteris FlexNoC cache coherent interconnect because of its design flexibility and market leading power, performance and area results. Using FlexNoC interconnect IP will allow us to get exactly the type of interconnect that we need for our SoCs, backed up by strong local support."*

Iluvatar-CoreX企业Logo
*Yunpeng Li, Chairman and CEO, **Iluvatar CoreX***

“We chose the Arteris FlexNoC cache coherent interconnect because of its design flexibility and market leading power, performance and area results,” said Yunpeng LI, Iluvatar CoreX Chairman and CEO. “Using FlexNoC interconnect IP will allow us to get exactly the type of interconnect that we need for our SoCs, backed up by strong local support.”

“We are excited to support Iluvatar CoreX for their deep learning SoC application ,” said K. Charles Janac, President and CEO of Arteris IP. “We look forward to a long cooperation as Iluvatar CoreX grows its exciting business opportunity.”

About Arteris IP

Arteris IP provides network-on-chip (NoC) interconnect IP to accelerate system-on-chip (SoC) semiconductor assembly for a wide range of applications from AI to automobiles, mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Samsung, Huawei / HiSilicon, Mobileye, and Texas Instruments. Arteris IP products include the Ncore cache coherent and FlexNoC non-coherent interconnect IP, the CodaCache standalone last level cache, and optional Resilience Package (ISO 26262 functional safety) and PIANO automated timing closure capabilities. Customer results obtained by using the Arteris IP product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at https://www.linkedin.com/company/arteris.

Editorial Contact

Kurt Shuler
Arteris IP
+1 408 470 7300
kurt.shuler@arteris.com