



## Arteris IP FlexNoC Interconnect Licensed by Silicon Mobility for OLEA ISO 26262 ASIL-D Automotive FPCU

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NoC interconnect supports functional safety data protection mechanisms of automotive chips

CAMPBELL, Calif. —March 12, 2019 —Arteris IP, the world's leading supplier of innovative, silicon-proven [network-on-chip \(NoC\) interconnect](#) intellectual property, today announced that Silicon Mobility has licensed [Arteris FlexNoC interconnect IP](#) for use in its range of [OLEA®FPCU](#) products as part of its SILant®ASIL-D functional safety integrated architecture.

*"Arteris FlexNoC interconnect IP meets our stringent requirements for on-chip functional safety data protection with extremely low latencies. As demonstrated with the first generation of FPCU, stunningly fast functional safety mechanisms bring significant benefits in applications such as electrified powertrains where risk margins can be reduced to push further the capability of a system. In this context, integration of FlexNoC will contribute to keeping Silicon Mobility OLEA products ahead in system safety."*



*Bruno Paucard, President and CEO, **Silicon Mobility***

Silicon Mobility pioneered the Field Programmable Control Unit (FPCU) chip, which provides a unique hardware and software programmability architecture with rich functional safety features for the control of critical automotive applications. The family of OLEA FPCU products is designed to meet the highest level of integrity with fault protection at the system level and unprecedented fault detection time, containment, and correction. The Arteris IP FlexNoC interconnect is used to connect IP blocks within the chip and protect the data communications between them.

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"Arteris FlexNoC interconnect IP meets our stringent requirements for on-chip functional safety data protection with extremely low latencies," said Bruno Paucard, President and CEO of Silicon Mobility. "As demonstrated with the first generation of FPCU, stunningly fast functional safety mechanisms bring significant benefits in applications such as electrified powertrains where risk margins can be reduced to push further the capability of a system. In this context, integration of FlexNoC will contribute to keeping Silicon Mobility OLEA products ahead in system safety."

"The Arteris IP team is excited that Silicon Mobility has chosen Arteris FlexNoC interconnect IP as the communications backbone of their OLEA ISO 26262 ASIL-D products," said K. Charles Janac, President and CEO of Arteris IP. "Arteris IP is the only IP company continually providing unique functional safety technologies that increase diagnostic coverage for our customers' chip designs, thereby ensuring an easier path to ISO 26262 compliance."

### **About Silicon Mobility**

Silicon Mobility is a full stack technology player powering control solutions for a cleaner, safer and smarter mobility. The company designs, develops and offers flexible, real-time, safe, and open semiconductor solutions used to increase energy efficiency and reduce pollutant emissions while keeping passengers safe. Silicon Mobility's products control electric motors, battery and energy management systems of electric and hybrid vehicles. By using Silicon Mobility's technologies, manufacturers improve the efficiency, reduce the size, weight, and cost of electric motors and increase the battery range and durability. Silicon Mobility technology accelerates the vehicle's powertrain electrification and the deployment of driverless vehicles for

OEMs. Silicon Mobility is headquartered in Sophia Antipolis, France with offices in Silicon Valley and Munich.

### **About Arteris IP**

Arteris IP provides [network-on-chip \(NoC\) interconnect IP](#) to accelerate system-on-chip (SoC) semiconductor assembly for a wide range of applications from AI to automobiles, mobile phones, IoT, cameras, SSD controllers, and servers for customers such as [Baidu](#), [Mobileye](#), [Samsung](#), [Huawei / HiSilicon](#), [Toshiba](#) and [NXP](#). Arteris IP products include the [Ncore](#) cache coherent and [FlexNoC](#) non-coherent interconnect IP, the [CodaCache](#) standalone last level cache, and optional [Resilience Package \(ISO 26262 functional safety\)](#), [FlexNoC AI Package](#), and [PIANO automated timing closure](#) capabilities. Customer results obtained by using Arteris IP products include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit [www.arteris.com](http://www.arteris.com) or find us on LinkedIn at <https://www.linkedin.com/company/arteris>.

### **Editorial Contact**

Kurt Shuler  
Arteris IP  
+1 408 470 7300  
[kurt.shuler@arteris.com](mailto:kurt.shuler@arteris.com)

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