



Silicon-Proven Arteris IP Ncore[®] Cache Coherent Interconnect Implemented in Toshiba ISO 26262-Compliant ADAS Chip

June 11, 2019

Toshiba tapes out next-generation automotive ADAS system-on-chip (SoC) using mature network-on-chip interconnect technology

CAMPBELL, Calif. — June 11, 2019 — Arteris IP, the world's leading supplier of innovative, silicon-proven [network-on-chip \(NoC\) interconnect](#) semiconductor intellectual property, today announced that Toshiba has taped out its next generation automotive advanced driver assistance system (ADAS) chip using the [Arteris IP Ncore Cache Coherent](#) and [FlexNoC[®] non-coherent interconnect](#) with the associated [Resilience Package](#).

"Our use of the uniquely flexible Ncore cache coherent interconnect IP helped us to more quickly design and implement our next generation automotive ADAS chips while allowing us to increase hardware diagnostic coverage for ISO 26262 compliance. The Arteris IP team was very helpful in guiding us on the interconnect configuration to optimize system performance and hardware diagnostic coverage using the integrated functional safety mechanisms. Working with the highly professional Arteris team and their world class interconnect IP has helped us meet our performance requirements and schedule, while adding valuable capabilities that would not be possible with other interconnects."

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Nobuaki Otsuka, Technology Executive at Electronic Device & Storage Corporation, Toshiba

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Toshiba's new ADAS SoC implements highly advanced image recognition and object detection using many processing engines and image processing accelerators working in parallel. Using the Ncore cache coherent interconnect allowed the Toshiba team to achieve better performance and smaller die area than their previous interconnect because of the Ncore IP's unparalleled flexibility. This state-of-the-art configurability for cache coherency enabled the interconnect to adapt to the chip layout and system-level requirements, rather than force the design team to "design around" a centralized interconnect. In addition, Toshiba took advantage of functional safety mechanisms within the interconnect IP to enhance the functional safety and overall diagnostic coverage of the chip, which helps facilitate ISO 26262 automotive safety integrity level (ASIL) compliance.

"Our use of the uniquely flexible Ncore cache coherent interconnect IP helped us to more quickly design and implement our next generation automotive ADAS chips while allowing us to increase hardware diagnostic coverage for ISO 26262 compliance," said Nobuaki Otsuka, Technology Executive at Toshiba Electronic Device & Storage Corporation. "The Arteris IP team was very helpful in guiding us on the interconnect configuration to optimize system performance and hardware diagnostic coverage using the integrated functional safety mechanisms. Working with the highly professional Arteris team and their world class interconnect IP has helped us meet our performance requirements and schedule, while adding valuable capabilities that would not be possible with other interconnects."

"We are excited that Toshiba has taped out their next-generation ADAS SoC using the Arteris IP Ncore Cache Coherent Interconnect," said K. Charles Janac, President and CEO of Arteris IP. "The Arteris IP Ncore cache coherent interconnect has been used in over 10 chip designs with three so far having been taped out or manufactured in engineering samples. About half of these SoC designs use the functional safety mechanisms for ISO 26262 compliance, provided by the Ncore Resilience Package."

About Arteris IP

Arteris IP provides [network-on-chip \(NoC\) interconnect IP](#) to accelerate system-on-chip (SoC) semiconductor assembly for a wide range of applications from AI to automobiles, mobile phones, IoT, cameras, SSD controllers, and servers for customers such as [Baidu](#), [Mobileye](#), [Samsung](#), [Huawei / HiSilicon](#), [Toshiba](#) and [NXP](#). Arteris IP products include the [Ncore[®]](#) cache coherent and [FlexNoC[®]](#) non-coherent interconnect IP, the [CodaCache[®]](#) standalone last level cache, and optional [Resilience Package \(ISO 26262 functional safety\)](#), [FlexNoC AI Package](#), and [PIANO[®] automated timing closure](#) capabilities. Customer results obtained by using Arteris IP products include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at <https://www.linkedin.com/company/arteris>.

Editorial Contact

Kurt Shuler

Arteris Inc.

+1 408 470 7300

kurt.shuler@arteris.com

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