Arteris Accelerates Industry Transition to Multi-Die Chiplet-Based Architecture

September 15, 2026

Expanded solution includes new FlexGen Multi-Die product to address the challenge of efficient data movement for an industry that is shifting to multi-die architectures, while preserving quality of service and architectural flexibility across chip boundaries

CAMPBELL, Calif., Sept. 15, 2026 (GLOBE NEWSWIRE) -- Arteris, Inc. (Nasdaq: AIP), a leading provider of semiconductor technology for accelerating innovation in the AI era, today announced an expansion of its multi-die portfolio that helps semiconductor companies transition from monolithic system-on-chip (SoC) designs to chiplet-based architectures for AI, HPC and consumer electronics applications, without having to reinvent how data moves through the system.

Semiconductor companies are increasingly adopting multi-die architectures to address the demands of AI computing. They are now building systems that extend beyond the practical size limits of a single die, optimizing individual chiplets for different process technologies and dividing a system across multiple dies. This introduces a new challenge: communication that previously occurred within one SoC must now cross physical chip boundaries, while maintaining performance, efficiency, and predictable traffic behavior.

Arteris addresses this challenge by extending network-on-chip (NoC) connectivity and data movement transparently across die-to-die links, allowing multiple dies to operate as a unified architecture. The new FlexGen Multi-Die product expands this approach for non-coherent AI and high-performance computing architectures and complements Ncore Multi-Die for cache-coherent systems.

Together with Arteris Magillem integration automation and Cycuity hardware security assurance, the expanded portfolio provides semiconductor engineering teams with technologies spanning data movement, system integration, and security for increasingly complex multi-die designs.

“Multi-die architectures represent one of the most important changes in semiconductor design since the introduction of the SoC itself,” said K. Charles Janac, president and CEO of Arteris. “As systems expand beyond the boundaries of a single piece of silicon, the challenge is no longer simply connecting chiplets; it is preserving the intelligence of the architecture across them. Our goal is to help engineering teams gain the benefits of multi-die architectures without having to reinvent the system every time they divide it across another piece of silicon.”

Extending NoC interconnect technology across chip boundaries

In a monolithic SoC, NoC technology serves as the fabric that enables processors, memory subsystems, accelerators and other functions to communicate and share data. Moving to a multi-die architecture creates physical boundaries between those functions, potentially requiring engineering teams to define and manage additional interfaces between chiplets.

Arteris extends NoC connectivity transparently across those boundaries, without reinventing the system. The new FlexGen Multi-Die NoC IP supports bidirectional transactions over a single UCIe PHY, reducing PHY area, power and I/O requirements by up to 50%. This approach allows engineering teams to preserve important NoC capabilities across die-to-die links, rather than treating each chiplet boundary as a separate system integration problem.

FlexGen Multi-Die is designed for non-coherent AI and HPC architectures and supports virtual channel link technology to improve utilization of limited chiplet I/O resources and advanced quality-of-service (QoS) mechanisms that maintain throughput for high-priority traffic across shared die-to-die links. These capabilities help engineering teams use available bandwidth efficiently, while scaling designs across multiple dies.

The broader Arteris multi-die portfolio includes:

- **FlexGen Multi-Die** for non-coherent AI and HPC architectures, extending efficient data movement and QoS capabilities across die boundaries.
- **Ncore Multi-Die** for cache-coherent compute architectures, enabling coherent connectivity and efficient data sharing across multiple dies.
- **Magillem integration automation**, which helps automate IP packaging, chiplet and multi-die integration, and hardware/software integration to reduce engineering effort and development complexity.
- **Cycuity hardware security assurance***, which helps engineering teams identify vulnerabilities earlier in development and verify security requirements across increasingly complex multi-die systems.

Together, these capabilities give semiconductor companies a more evolutionary path from monolithic SoCs to multi-die architectures, while helping engineering teams improve design reuse, reduce integration complexity and bring differentiated products to market faster.

From monolithic designs to multi-die products

Arteris customers are already using the company's technology as they transition existing architectures from single-die implementations to multi-die products.

"As Agentic AI workloads continue to expand across cloud infrastructure, edge and endpoint devices, multi-die architectures are becoming increasingly important for balancing performance, scalability, and development efficiency," said Jason Miller, senior director, Silicon Design at AMD.

"Solutions that simplify system integration, while preserving bandwidth and performance across chiplets, help engineering teams accelerate innovation and bring differentiated products to market faster. Arteris' continued expansion of its multi-die portfolio supports the flexibility and productivity required for our next generation of data center, client, gaming, and embedded compute products."

"The future of advanced semiconductor design is inherently multi-die" said Daisuke Murakami, executive chief engineer, Global Leading Group at Socionext. "By collaborating with Arteris on its UCIe-based multi-die solution, we gain early access to technologies that simplify chiplet integration while enabling the scalability, bandwidth and efficiency needed for next-generation AI, automotive and data-center SoCs."

Building toward a broader chiplet ecosystem

As multi-die adoption expands, interoperability among NoC technologies, die-to-die interfaces, chiplet IP, design tools and advanced packaging technologies will become increasingly important. Arteris is working with semiconductor IP and ecosystem partners to help reduce integration risk and establish more reusable foundations for multi-die design.

“Physical AI systems require right-sized inference and scalable architectures that seamlessly integrate diverse compute technologies while meeting stringent power, performance, safety, security, and reliability requirements,” said David Glasco, vice president of R&D, Silicon Solutions Group at Cadence. “By combining the comprehensive Cadence Physical AI platform, IP, and security solutions with Arteris’ NoC IP, our collaboration enables accelerated silicon realization and trusted system deployment from cloud to edge. This reusable foundation helps customers scale physical AI systems more efficiently, reduce development risk, and speed time to market. Together, Cadence and Arteris provide a seamless path from specification to silicon to deployment, accelerating innovation across the physical AI ecosystem.”

“An open chiplet ecosystem requires architectural frameworks that simplify the integration of specialized dies into scalable, manufacturable systems,” said Suresh Subramaniam Ph.D., CTO, systems and advanced packaging at Silitronics. “We plan to leverage Arteris FlexGen technology in our development of an OCP-derived chiplet architecture, combining intelligent die-to-die connectivity with Silitronics’ system-level design, advanced packaging and heterogeneous integration capabilities to help customers bring differentiated multi-die solutions to market faster.”

“As multi-die designs become increasingly central to AI and high-performance computing innovation, interoperability across the chiplet ecosystem is critical to reducing design complexity and accelerating adoption,” said Neeraj Paliwal, senior vice president of product management at Synopsys. “The successful validation of interoperability between Synopsys' silicon-proven UCIe IP, delivering high-bandwidth, low-latency die-to-die connectivity, and Arteris Ncore Cache Coherent NoC IP for multi-die designs helps customers confidently integrate chiplets, reduce integration risk, and enable silicon success.”

“UCIe provides an open, high-performance foundation for integrating chiplets across different functions and process technologies,” said Mao Liu, vice president at UniVista. “By working with Arteris to validate interoperability between UniVista UCIe IP and Arteris Ncore Multi-Die, we aim to provide customers with a more integrated path to scalable, cache-coherent multi-die designs for AI, high-performance computing and other compute-intensive applications.”

A practical path to the chiplet future

AI compute systems of the future require the transparent data movement solutions that Arteris is bringing to the industry, to speed the development and delivery of advanced heterogeneous systems. The new FlexGen Multi-Die product transparently extends non-coherent connectivity across die boundaries, enabling engineering teams to address different connectivity requirements across future multi-die SoC implementations.

The expanded Arteris multi-die solution is available today to early access partners and strategic customers. Learn more at arteris.com/multi-die.

About Arteris

Arteris is a leading provider of semiconductor technology that accelerates the creation of high-performance, power-efficient silicon with built-in safety, reliability, and security. Innovative Arteris products are designed to optimize data movement and help ease complexity in the modern AI era with network-on-chip (NoC) interconnect intellectual property (IP), system-on-chip (SoC) software for integration automation and hardware security assurance. All are used by the world's top technology companies to improve overall performance and engineering productivity, reduce risk, lower costs, and bring cutting-edge designs to market faster. Learn more at arteris.com.

*Not available in all markets.

Forward-Looking Statements
This press release contains forward-looking statements within the meaning of the Private Securities Litigation Reform Act of 1995, including statements regarding the Company’s expectations, plans, objectives, outlook, projected financial or operating results, market opportunities, product development, and/or business strategy. These statements are based on management’s current expectations, estimates, assumptions, and projections and are not historical facts. Words such as “may,” “will,” “could,” “would,” “expect,” “anticipate,” “believe,” “estimate,” “plan,” “intend,” “project,” “potential,” and similar expressions are intended to identify forward-looking statements.

These statements are subject to risks and uncertainties that could cause actual results to differ materially from those expressed or implied, including economic and market conditions; supply-chain constraints; technological developments; regulatory changes; litigation; cybersecurity risks; availability of capital; and other risks. Additional information regarding these and other risks is included in the Company’s filings with the Securities and Exchange Commission.

The forward-looking statements speak only as of the date of this press release. The Company undertakes no obligation to update or revise any forward-looking statement, except as required by applicable law.

Media Contact:
Gina Jacobs

Arteris
+1 408 560 3044
newsroom@arteris.com