Arteris Addresses Silicon Design Reuse Challenge with New Magillem Packaging Product for IP Blocks and Chiplets

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CAMPBELL, Calif., June 23, 2025 (GLOBE NEWSWIRE) -- Arteris, Inc. (Nasdaq: AIP), a leading provider of system IP for accelerating semiconductor creation, today announced the immediate availability of Magillem Packaging, a new software product designed to simplify and speed up the process of building advanced chips used in everything from AI data centers to edge devices.

As chip design becomes increasingly complex with more components, higher performance demands and tighter timelines, Magillem Packaging helps engineering teams work faster and more efficiently by automating one of the most time-consuming parts of the design process: assembling and reusing existing technology.

“The soaring count of silicon IP blocks, expanding AI compute, scaling of subsystem IPs, and rapid growth of chiplets are all driving unprecedented integration challenges in semiconductor design,” said K. Charles Janac, president and CEO of Arteris. “Magillem Packaging streamlines this complexity, automating IP readiness and assembly to boost productivity and help our partners and customers deliver advanced technologies faster.”

Magillem Packaging enables IP teams to quickly and reliably package and prepare hundreds or even thousands of components for integration into a chiplet or SoC, including new, existing or third-party IP blocks. Based on the latest version of the IEEE 1685 (IP-XACT) standard, Magillem Packaging works seamlessly with industry tools and silicon IP, helping companies keep up with increasing design demands while reducing costly errors and delays.

Key Capabilities of Magillem Packaging from Arteris:

- **IP Reuse** with comprehensive IP, subsystem and chiplet packaging in a reusable format including configuration, implementation and verification for incremental and full packaging with a proven methodology.
- **Correct-by-construction IEEE 1685-2022 generation** without requiring any pre-requisite IP-XACT expertise, while standard compliance and data consistency are ensured by construction and assessed with a built-in Magillem checkers suite.
- **Scalable and fully automated** generation of IP packaging for both reused and new IP blocks, with support for legacy 2009 and 2014 versions of IEEE 1685 standard, with intuitive graphical editors enabling fast viewing and editing of IP block descriptions.

The new software builds on Arteris’ proven approach to design automation and complements its broader suite of products used by many of the world’s top semiconductor companies.
Learn more at arteris.com/MagillemPackaging.

“Andes Technology is recognized for our comprehensive family of RISC-V processor IP and customization tools that empower customers to easily differentiate their SoC designs,” said Marc Evans, director of business development & marketing at Andes Technology Corporation. “The latest IP-XACT 2022 specifications enable structured automation, optimizing IP packaging and integration. Magillem Packaging complements Andes’ commitment to streamlined workflows, enabling faster and more reliable SoC development.”

"The MIPS Atlas portfolio is engineered for high-efficiency compute in autonomous, industrial, and embedded AI applications, where rapid integration and design reuse are critical," said Drew Barbier, VP & GM of the IP Business Unit at MIPS. "Arteris Magillem Packaging, with its automation of IP-XACT 2022-compliant packaging and support for industry standards, aligns with customer needs to accelerate SoC development. Together, we empower customers to streamline IP integration, reduce design complexity, and bring innovative silicon to market faster."

About Arteris
Arteris is a global leader in system IP used in semiconductors to accelerate the creation of high-performance, power-efficient silicon. Arteris network-on-chip (NoC) interconnect IP and system-on-chip (SoC) integration automation software are used by the world's top semiconductor and technology companies to improve overall performance, engineering productivity, reduce risk, lower costs, and bring complex designs to market faster. Learn more at arteris.com.

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