



Arteris Accelerates AI-Driven Silicon Innovation with Expanded Multi-Die Solution

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CAMPBELL, Calif., June 17, 2025 (GLOBE NEWSWIRE) -- In a market reshaped by the compute demands of AI, Arteris, Inc. (Nasdaq: AIP), a leading provider of system IP for accelerating semiconductor creation, today announced an expansion of its multi-die solution, delivering a foundational technology for rapid chiplet-based innovation.

"In the chiplet era, the need for computational power increasingly exceeds what is available by traditional monolithic die designs," said K. Charles Janac, president and CEO of Arteris. "Arteris is leading the transition into the chiplet era with standards-based, automated and silicon-proven solutions that enable seamless integration across IP cores, chiplets, and SoCs."

Moore's Law, predicting the doubling of transistor count on a chip every two years, is slowing down. As the semiconductor industry accelerates efforts to increase performance and efficiency, especially driven by AI workloads, architectural innovation through multi-die systems has become critical. Arteris' expanded multi-die solution addresses this shift with a suite of enhanced technologies that are purpose-built for scalable and faster time-to-silicon, high-performance computing, and automotive-grade mission-critical designs.

Business Impact: From Innovation to Market Acceleration

Arteris' offering reduces chiplet and SoC design time, along with the optimization of power, performance, and area bottlenecks by providing key Network-on-Chip (NoC) IP technology for standardized die-to-die communication and automating key SoC creation workflows.

Built for interoperability, the expanded solution supports the Universal Chiplet Interconnect Express (UCIe) specification, various Arm AMBA protocols, PCIe, and integration with leading physical IPs to ensure robust, standards-based ecosystem compatibility. Integration with products from major EDA and foundry partners — Cadence, Synopsys and global fabs — ensures a ready-to-deploy solution for silicon innovators and system companies creating electronics.

Key Capabilities of the Arteris Multi-Die Solution:

- **Silicon-proven non-coherent FlexNoC IP** supports the relevant standards and integrates with third-party commercially available die-to-die controllers and PHYs.
- **New cache-coherent Ncore NoC IP capabilities** enabling seamless cache coherent reads and writes across multiple chiplets, making multi-die systems look like a single piece of silicon to application software programmers.
- **Optimized Magillem Connectivity** automation for SoC assembly from IP and chiplets, reducing project risks associated with manual, error-prone integration tasks.
- **Optimized Magillem Registers** automation for integrating hardware and software from system map definition to validation and documentation based on a single source of truth.

Strategic Momentum

As part of their focus on supporting chip architecture across the board, Arteris is collaborating with leading players across the silicon value chain to enable next-generation AI and automotive platforms:

- **Arm** is collaborating with Arteris to enable an interoperable chiplet ecosystem via the recent AMBA CHI C2C specification and the ongoing support of mutual automotive semiconductor customers, Tier 1s and OEMs.
- **Cadence** is collaborating with Arteris to enable customers to realize their chiplet ambitions through integrated, optimized, standards-compliant IP and EDA tool flows, delivering significant time-to-market acceleration while reducing development costs.
- **Renesas** is leveraging Arteris multi-die technology in its R-Car Gen 5 SoC platform for advanced driver-assistance systems (ADAS) that integrate CPUs, AI-enabled NPU, IVI-enabled GPUs, and ability to further boost AI throughput via chiplet extensions.
- **RISC-V ecosystem partners** like Andes, SiFive and Tenstorrent are working with Arteris in support of domain-specific IPs and chiplets.
- **Synopsys** is collaborating with Arteris to enable fast integration with a portfolio of standards-compliant IP and EDA solutions for multi-die designs.

"The rapid pace of technological innovation and the growing demand for advanced physical AI silicon are redefining SoC designs, which are shifting from monolithic to chiplet-based architectures," said David Glasco, vice president of R&D, Silicon Solutions Group at Cadence. "By collaborating with Arteris, we're accelerating the journey to chiplet-based systems, optimizing key performance metrics and ensuring seamless multi-die interoperability. Together, we're not just enabling the chiplet marketplace ecosystem — we're pioneering its future."

"As AI pushes the limits of performance and power efficiency, monolithic SoCs with chiplet capabilities have become essential in delivering the integration and scalability that traditional SoC designs can't match," said Aish Dubey, vice president and general manager, Digital High Performance Computing SoC Business at Renesas. "Arteris technology plays a key role in realizing this vision by providing the underlying connectivity in our 5th generation R-Car automotive silicon and driving the new era of automotive innovation."

"Our companies have enjoyed a multi-year collaboration centered on reducing the risk, development cost and timeline for customers that wish to use our respective products to create best-in-class, scalable platforms," said Ian Ferguson, VP, vertical markets at SiFive. "SiFive views Arteris' multi-die announcement as a very natural extension to this collaboration and is firmly committed to placing its support in achieving its success from both technical and business perspectives."

"The adoption of multi-die design to meet the growing computational demands of AI and HPC applications is well underway, necessitating the focus on ecosystem collaboration for cutting-edge solutions," said Neeraj Paliwal, senior vice president of product management at Synopsys. "Synopsys UCle IP, silicon-proven in several customer designs, interoperates with Arteris' NoC IP to deliver high performance while providing standards-based solutions. Available IP models in Synopsys Platform Architect enable early architecture exploration, accelerating the development of multi-die designs."

"Member company innovation in chiplet design using UCle IP is essential for broad ecosystem interoperability," added Dr. Debendra Das Sharma, chairman, at UCle Consortium. "Arteris' advancements strengthen the foundation for the next generation of open, scalable silicon based on UCle."

Why This Matters Now

Advanced semiconductor capabilities are vital for the development of future AI solutions and Arteris' innovative technology plays a pivotal role. The expanded multi-die solution allows semiconductor firms to compress development cycles, scale modular architectures, and deliver differentiated AI performance — while staying aligned with evolving industry realities.

The expanded Arteris multi-die solution is available now to early access partners. Learn more at arteris.com/multi-die.

About Arteris

Arteris is a global leader in system IP used in semiconductors to accelerate the creation of high-performance, power-efficient silicon. Arteris network-on-chip (NoC) interconnect IP and system-on-chip (SoC) integration automation software are used by the world's top semiconductor and technology companies to improve overall performance, engineering productivity, reduce risk, lower costs, and bring complex designs to market faster. Learn more at arteris.com.

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Media Contact:

Gina Jacobs
Arteris
+1 408 560 3044
newsroom@arteris.com

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