Arteris Releases the Latest Generation of Magillem Registers to Automate Semiconductor Hardware/Software Integration

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Highlights:

- **Solution Integration:** Integration of acquired silicon-proven Magillem 5 and Semifore CSRCompiler products into a next-generation ‘single source of truth’ software product for register management and Hardware/Software Interface automation.
- **Any Design:** Up to 3x expanded performance and 5x scalability address today’s SoCs and FPGA designs, ranging from simple IoT devices to state-of-the-art complex AI SoCs.
- **Broad Standards Support:** Augments existing support of IEEE 1685-2009 (IP-XACT) standard with support of the 2014 and 2022 versions, and that of Accellera SystemRDL standard with SystemRDL 2.0 for better hardware/software integration.

CAMPBELL, Calif., Feb. 25, 2025 (GLOBE NEWSWIRE) -- Arteris, Inc. (Nasdaq: AIP), a leading provider of system IP which accelerates system-on-chip (SoC) creation, today announced the immediate availability of the latest generation of Magillem Registers technology for SoC integration automation. This product enables design teams to automate the hardware/software integration process, reducing the development time by 35% when compared to in-house solutions and empowers them to overcome design complexity challenges, freeing up cycles for new innovation.

Magillem Registers is a comprehensive register design and management product that accurately automates the hardware/software interface (HSI) to quickly develop chips and chiplets ranging from IoT devices to complex AI datacenter multi-die SoCs. This product empowers chip architects, hardware designers, firmware engineers, verification teams, and documentation teams to overcome complexity and satisfy the need for real-time, effective cross-functional team communication. It mitigates the risk of out-of-date standards with a unified specification and compilation flow to generate accurate designs.

Building upon the silicon-proven Magillem 5 and CSRCompiler technologies, the latest release of Magillem Registers is designed to streamline and optimize workflows by providing an integrated, single source of truth infrastructure to specify, document, implement, and verify SoC address maps. This approach boosts productivity by promoting efficient IP reuse and ensuring consistency across the relevant design teams. With over 1,000 semantic and syntactic checks, Magillem Registers ensures high-quality output, validating third-party IPs, in-house IPs, and overall system integration to significantly reduce the risk of silicon failure. Additionally, intelligent automation enables a remarkable 35%-time reduction in HSI development compared to manual solutions, empowering development teams to meet tight deadlines with confidence.

The latest release of Magillem Registers brings significant advancements to performance, capacity, standards support, and usability. It delivers up to 3x faster performance compared to Magillem 5, enabling the compilation of millions of registers within minutes while auto-generating synthesizable RTL register banks. With a 5x increase in supported design size, it scales seamlessly from small to very large multi-die devices which contain millions of control registers.

Magillem Registers offers broad support for industry standards, including the addition of IEEE 1685-2022 (IP-XACT) and SystemRDL 2.0, alongside the previous versions. This enhances intellectual property (IP) reuse, and expands compatibility with third-party IP vendors, improving SoC integration. Usability enhancements further boost team productivity with a rapid, highly iterative design environment incorporating features for streamlined input, intuitive document navigation, customizable workflows, and the elimination of repetitive time-consuming and error-prone manual tasks through advanced automation. Magillem Registers addresses the growing demands of modern design environments with unmatched efficiency and scalability.

“With over 70% of chips requiring respins, effectively addressing hardware and software integration has become quite a challenge for SoC teams, particularly given added complexity and growing chip sizes driven by the infusion of AI logic,” said K. Charles Janac, president and CEO of Arteris. “Building AI SoCs and FPGAs is expensive and time-consuming, so automation efficiencies are critical to cost control and our latest release of Magillem Registers ensures that SoC engineering productivity is maximized, and project risks are significantly reduced.”

Arteris’ SoC integration automation products, including Magillem Registers, are designed to automate around complexity, liberate team productivity, and accelerate quality chiplet and SoC design flows. For more information please visit arteris.com/magillem-registers.

About Arteris

Arteris is a leading provider of system IP for accelerating system-on-chip (SoC) development across today’s electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration automation technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

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Media Contact:
Gina Jacobs

Arteris
+1 408 560 3044
newsroom@arteris.com

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